CLAIMS

1. A current source circuit adapted to provide at an output an output current defined by an average of ratios of measurement currents, each ratio provided by a plurality of (N+1) equivalent current sources coupled in common to a current output, the first term of each ratio being defined by a selected one of the plurality of current sources and the second term of each ratio being defined by the remaining current sources of the plurality of current sources, and wherein the current source circuit is further adapted to enable a selective changing of the one of the plurality of current sources providing the first term until each of the N+1 current sources has, in turn, provided the first term, the output current being equivalent to the average of the sum of ratios so determined.

2. A temperature measurement circuit comprising a plurality of (N+1) equivalent current sources, each of the current sources being individually switchable to at least one transistor, the current sources being arranged to generate a PTAT voltage at the output of the at least one transistor, the PTAT voltage being defined by an applied current coupled to the at least one transistor and being representative of the temperature measured by the circuit, the applied current being provided by a ratio of the N+1 current sources, and wherein the first term of the ratio is provided by a selected one of the plurality of current sources and the second term of the ratio is provided by the remaining current sources of the plurality of current sources.

3. The circuit as claimed in claim 2 being further adapted to enable a selective changing of the one of the plurality of current sources providing the first term of the ratio.

4. The circuit as claimed in claim 3 being further adapted to enable a shuffling through the N+1 current sources to change the selected one of the current sources providing the first term of the ratio, thereby sequentially coupling a plurality of applied currents, each defined by a ratio of the N+1 current sources, to the at least one transistor.

5. The circuit as claimed in claim 4 being further adapted to effect the shuffling of the current sources until each of the N+1 current sources has, in turn, provided the first term of the ratio.

6. The circuit as claimed in claim 5, further including storage circuitry adapted to store a value representative of the generated voltage for each of the shuffled ratios.

7. The circuit as claimed in claim 6 further including a digitizer, the digitizer adapted to digitise the voltage such that each of the values representative of the generated voltage is a digital word.

8. The circuit as claimed in claim 6 further including averaging components adapted to define an average value for the stored values representative of the voltage determined in each of the sequential coupling steps.

9. The circuit as claimed in claim 2 wherein the number (N+1) of current sources provided is determined by the value of 2^n, where n>1.

10. The circuit as claimed in claim 9 where n is selected from one of 3, 4, or 5.

11. The circuit as claimed in claim 10 wherein n is equal to 4.

12. The circuit as claimed in claim 2 wherein the circuitry is defined on a single chip and the chip further includes circuitry adapted to couple a voltage defined by the base emitter voltage of the at least one transistor to a pin providing external access to the chip, the voltage being externally measurable at that external pin, thereby enabling an external calibration of the temperature sensed on-chip.

13. The circuit as claimed in claim 12 wherein two transistors are provided and two pins are provided, the circuit being adapted to couple a voltage defined by the base emitter voltage of each transistor to a corresponding pin, thereby enabling an external evaluation of the PTAT voltage generated by the difference between the two base emitter voltages.

14. The circuit as claimed in claim 12 wherein the pin is provided with dual functionality such that when the pin is providing the external calibration of the temperature it adopts a first level of functionality and in normal operation of the circuit the pin has a second level of functionality.

15. The circuit as claimed in claim 2 wherein the at least one transistor is provided by a bipolar junction transistor.

16. The circuit as claimed in claim 2 wherein the at least one transistor is provided in a CMOS implementation, the transistor being provided by a parasitic transistor.

17. The circuit as claimed in claim 2 wherein two transistors are provided, each transistor being individually switchable to each of the plurality of N+1 current sources and wherein through a sequential coupling of each of the transistors to either one of the current sources or the remaining of the current sources a voltage which is proportional to absolute temperature may be obtained.

18. The circuit as claimed in claim 2 wherein two transistors are provided, each transistor being adapted to provide a PTAT voltage, the PTAT voltage of the first transistor being out of phase with that of the second transistor.

19. The circuit as claimed in claim 18 being adapted such that, in use, at any one instant the first term of the ratio is coupled to the first transistor and the second term of the ratio is coupled to the second transistor.

20. A temperature sensor chip having:

a first set of circuitry providing at an output a temperature dependent (PTAT) voltage,

a second set of circuitry adapted to digitize the PTAT voltage,

a third set of circuitry adapted to store and average a plurality of digitized PTAT voltages, thereby providing at an output of the chip a digitized averaged measurement value representative of the temperature on the chip, and wherein

the first set of circuitry includes a current source array and at least one transistor, the PTAT voltage being defined by a coupling of a ratio of the currents provided from the current source array to the at least one transistor, the ratio being defined by a first term equivalent to one of the current sources of the array and a second term equivalent to the remainder of the current sources of the array, and further wherein the plurality of PTAT voltages are defined by shuffling through the current source array so as to sequentially vary the ratio coupled to the at least one transistor.

21. The chip as claimed in claim 20 further including a fourth set of circuitry, the fourth set of circuitry being adapted to couple an output from the first set of circuitry to at least one pin provided on the chip, thereby providing a set of measured voltages at that pin, the measured voltages being externally measurable using an external set of circuitry which may be coupled to that pin.

22. A method of sensing and measuring temperature on a chip, the method comprising the steps of:

providing a first set of circuitry adapted to provide a voltage representative of the temperature on the chip,

providing a second set of circuitry adapted to digitise the voltage,

providing a third set of circuitry adapted to store and average a plurality of digitised voltages, thereby providing at an output of the chip a digitised averaged measurement value representative of the temperature on the chip, and wherein

the first set of circuitry includes a current source array and at least one transistor, the voltage being provided by a coupling of an applied current defined by a ratio of the currents provided from the current source array to the at least one transistor, the ratio being defined by a first term equivalent to one of the current sources of the array and a second term equivalent to the remainder of the current sources or the array, and further wherein the plurality of voltages are defined by the step of shuffling through the current source array so as to sequentially vary the ratio coupled to the at least one transistor.